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**1 Patient management systems: the early years**

W. E. Hammond

December 1987 Proceedings of ACM conference on History of medical informatics

Publisher: ACM

Full text available: Pdf (880.60 KB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [index to](#)

Bibliometrics: Downloads (6 Weeks): 27, Downloads (12 Months): 299, Citation Count: 0

As I scanned through old papers and reports in preparation for these remarks, I became in the "sameness" of those proposals and descriptions with what is happening today. There are major differences - today's systems ...

**2 Test strategies for low power devices**

C. P. Ravikumar, M. Hirech, X. Wen

 March 2008 DATE '08: Proceedings of the conference on Design, automation and test in E  
 Publisher: ACM

Full text available: Pdf (356.97 KB)

 Additional Information: [full citation](#), [abstract](#), [references](#)

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 28, Citation Count: 0

Ultra low-power devices are being developed for embedded applications in bio-medical wireless sensor networks, environment monitoring and protection, etc. The testing of low-power devices is a daunting task. Depending on ...

**3 Energy-aware design of embedded memories: A survey of technologies, architecture optimization techniques**

Luca Benini, Alberto Macii, Massimo Poncino

 February 2003 Transactions on Embedded Computing Systems (TECS) . Volume 2 Issue  
 Publisher: ACM



Full text available: Pdf (288.44 KB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [cited by](#)

Bibliometrics: Downloads (6 Weeks): 32, Downloads (12 Months): 229, Citation Count: 8

Embedded systems are often designed under stringent energy consumption budgets, generation and battery size. Since memory systems consume a significant amount of energy and to forward data, it is then imperative to balance power ...

**Keywords:** Embedded systems, embedded memories, integration, memories, nonvolatile on-a-chip, volatile

-  [VirtualPower: coordinated power management in virtualized enterprise systems](#)  
 Ripai Nathuji, Karsten Schwan  
 October 2007 SOSP '07: Proceedings of twenty-first ACM SIGOPS symposium on Operating systems principles  
 Publisher: ACM  
 Full text available:  Pdf (789.55 KB)      Additional Information: [full citation](#), [abstract](#), [references](#), [index to](#)  
 Bibliometrics: Downloads (6 Weeks): 45, Downloads (12 Months): 365, Citation Count: 4

Power management has become increasingly necessary in large-scale datacenters to a and limitations in cooling or power delivery. This paper explores how to integrate power management mechanisms and policies with the virtualization technologies ...

**Keywords:** power management, virtualization

Also published in:

October 2007 SIGOPS Operating Systems Review Volume 41 Issue 6

- 5 [Tailoring circuit-switched network-on-chip to application-specific system-on-chip b](#)  
 [optimization schemes](#)  
 Kuei-Chung Chang, Jih-Sheng Shen, Tien-Fu Chen  
 January 2008 Transactions on Design Automation of Electronic Systems (TODAES)  
 Publisher: ACM  
 Full text available:  Pdf (816.85 KB)      Additional Information: [full citation](#), [abstract](#), [references](#), [index to](#)  
 Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 154, Citation Count: 0


As the number of cores on a chip increases, power consumed by the communication st a significant portion of the overall power budget. In this article, we first propose a circi interconnection architecture which uses *crossroad* ...

**Keywords:** Application specific, interconnection, low power, networks on chip, system


- 6 [A critical-path-aware partial gating approach for test power reduction](#)  
 Mohammed Elshoukry, Mohammad Tehranipoor, C. P. Ravikumar  
 April 2007 Transactions on Design Automation of Electronic Systems (TODAES) ,  
 Publisher: ACM  
 Full text available:  Pdf (628.17 KB)      Additional Information: [full citation](#), [abstract](#), [references](#), [index to](#)  
 Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 56, Citation Count: 0

Power reduction during test application is important from the viewpoint of chip reliabili obtaining correct test results. One of the ways to reduce scan test power is to block tr propagating from the outputs of scan cells through combinational ...

**Keywords:** Low-power testing, partial gating, scan cell gating, scan testing

- 7 [RL-huffman encoding for test compression and power reduction in scan applicatio](#)  
 Mehrdad Nourani, Mohammad H. Tehranipoor  
 January 2005 Transactions on Design Automation of Electronic Systems (TODAES)

<sup>1</sup>  
Publisher: ACM

Full text available:  Pdf (321.93 KB)


Additional Information: [full citation](#), [abstract](#), [references](#), [cited by](#)

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 80, Citation Count: 3

This article mixes two encoding techniques to reduce test data volume, test pattern de and power dissipation in scan test applications. This is achieved by using run-length er followed by Huffman encoding. This combination is especially ...


Keywords: Compression ratio, Huffman encoding, decompression, power reduction, ri encoding, scan applications, scan-in test power, switching activities, test compression, compression

<sup>8</sup> [A low-power SRAM using bit-line charge-recycling technique](#)

 Keesjong Kim, Hamid Mahmoodi, Kaushik Roy

August 2007 DATE '07: Proceedings of the 2007 international symposium on Low power and design

Publisher: ACM

Full text available:  Pdf (705.54 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index to](#)

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 94, Citation Count: 0

We propose a new low-power SRAM using bit-line Charge Recycling (CR-SRAM) for the operation. In the proposed write scheme, differential voltage swing of a bit-line is obtained by recycling charge from its adjacent bit-line capacitance. In order ...


Keywords: SRAM, charge-recycling, low power, process variation, write margin, write

<sup>9</sup> [Using the inter- and intra-switch regularity in NoC switch testing](#)

Mohammad Hosseinabady, Atefe Dalirsani, Zainatabedin Navabi

April 2007 DATE '07: Proceedings of the conference on Design, automation and test in E

Publisher: EDA Consortium


Full text available:  Pdf (288.77 KB)

Additional Information: [full citation](#), [abstract](#), [references](#)

Bibliometrics: Downloads (6 Weeks): 12, Downloads (12 Months): 56, Citation Count: 0


This paper proposes an efficient test methodology to test switches in a Network-on-Chip architecture. A switch in an NoC consists of a number of ports and a router. Using the regularity among ports of a switch and inter-switch regularity ...

<sup>10</sup> [A highly configurable cache for low energy embedded systems](#)

 Chuanjun Zhang, Frank Vahid, Walid Najjar

May 2005 Transactions on Embedded Computing Systems (TECS), Volume 4 Issue 2

Publisher: ACM

Full text available:  Pdf (714.89 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [cited by](#)

Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 71, Citation Count: 7

Energy consumption is a major concern in many embedded computing systems. Several studies have shown that cache memories account for about 50% of the total energy consumed by these systems. The performance of a given cache architecture is determined, ...

**Keywords:** Cache, architecture tuning, configurable, embedded systems, low energy, memory hierarchy, microprocessor

# 11 Power analysis of system-level on-chip communication architectures



Kanishka Lahiri, Anand Raghunathan

September 2004 CODES+ISSS '04: Proceedings of the 2nd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis

Publisher: ACM

Full text available: Pdf (101.16 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [cited by](#)

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 64, Citation Count: 5

For complex System-on-chips (SoCs) fabricated in nanometer technologies, the system communication architecture is emerging as a significant source of power consumption. optimizing this important component of SoC power requires ...

**Keywords:** communication architectures, low-power design, network-on-chip, power in system-on-chip

# 12 Low power Illinois scan architecture for simultaneous power and test data volume



Anshuman Chandra, Felix Ng, Rohit Kapur

March 2008 DATE '08: Proceedings of the conference on Design, automation and test in Europe Publisher: ACM

Full text available: Pdf (301.27 KB)

Additional Information: [full citation](#), [abstract](#), [references](#)

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 11, Citation Count: 0

We present Low Power Illinois scan architecture (LPILS) to achieve power dissipation a volume reduction, simultaneously. By using the proposed scan architecture, dynamic power dissipation during scan testing in registers and combinational ...

# 13 Architecting a reliable CMP switch architecture



Kypros Constantinides, Stephen Plaza, Jason Biome, Valeria Bertacco, Scott Mahlke, Todd Zhang, Michael Orshansky

March 2007 Transactions on Architecture and Code Optimization (TACO) . Volume 4 Issue 1 Publisher: ACM

Full text available: Pdf (593.20 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index to](#)

Bibliometrics: Downloads (6 Weeks): 12, Downloads (12 Months): 149, Citation Count: 0

As silicon technologies move into the nanometer regime, transistor reliability is expected. devices become subject to extreme process variation, particle-induced transient errors transistor wear-out. Unless these challenges are addressed, ...

**Keywords:** CMP switch, defect-tolerance, reliability

# 14 Communications of the ACM: Volume 51 Issue 8



August 2008 Communications of the ACM

Publisher: ACM

Full text available: Digital Edition , Pdf (6.85 MB) Additional Information: [full citation](#)

Bibliometrics: Downloads (6 Weeks): 427, Downloads (12 Months): 2220, Citation Count: 0

15 [A Technique to Reduce Peak Current and Average Power Dissipation in Scan Design with Limited Capture](#)

Seongmoon Wang, Wenlong Wei

January 2007 ASP-DAC '07: Proceedings of the 2007 conference on Asia South Pacific design automation

Publisher: IEEE Computer Society

Full text available:  Pdf (251.46 KB) Additional Information: [full citation](#), [abstract](#), [index terms](#)

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 28, Citation Count: 2

In this paper, a technique that can efficiently reduce peak and average switching activity application is proposed. The proposed method does not require any specific clock tree special scan cells, or scan chain reordering. Test ...

**Keywords:** ATPG, peak current reduction, average power dissipation, scan designs, clock construction, special scan cells, scan chain reordering

16 [Toward a scalable test methodology for 2D-mesh Network-on-Chips](#)

Kim Petersén, Johnny Öberg


April 2007 DATE '07: Proceedings of the conference on Design, automation and test in Europe Publisher: EDA Consortium

Full text available:  Pdf (232.31 KB) Additional Information: [full citation](#), [abstract](#), [references](#)

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 61, Citation Count: 0

This paper presents a BIST strategy for testing the NoC interconnect network, and inverse strategy is a suitable approach for the task. All switches and links in the NoC are tested running at full clock-speed, and in a functional-like ...

17 [An automated method for test model generation from switch level circuits](#)

 Tim McDougall, Atanas Parashkevov, Simon Jolly, Juhong Zhu, Jing Zeng, Carol Pyron, Ma

January 2003 ASPDAC: Proceedings of the 2003 conference on Asia South Pacific design automation Publisher: ACM

Full text available:  Pdf (116.62 KB) Additional Information: [full citation](#), [abstract](#), [references](#)

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 9, Citation Count: 0

Custom VLSI design at the switch level is commonly applied when a chip is required to stringent operating requirements in terms of speed, power, or area. ATPG requires gate models, which are verified for correctness against switch level models. ...

18 [A sophisticated memory test engine for LCD display drivers](#)

Oliver Spang, Hans-Martin von Staudt, Michael G. Wahl

April 2007 DATE '07: Proceedings of the conference on Design, automation and test in Europe Publisher: EDA Consortium

Full text available:  Pdf (884.68 KB) Additional Information: [full citation](#), [abstract](#), [references](#)

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 16, Citation Count: 0

Economic testing of small devices like LCD drivers is a real challenge. In this paper we approach where a production tester is extended by a memory test engine (MTE). This consists of hardware and software components allows testing ...

[Proceedings of the conference on Design, automation and test in Europe](#)

Rudy Lauwereins, Jan Madsen

April 2007 DATE '07: Proceedings of the conference on Design, automation and test in E  
Publisher: EDA ConsortiumAdditional Information: [full citation](#), [abstract](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citation Count: 0


Welcome to the DATE 07 Conference Proceedings. DATE combines the world's leading systems design conference and Europe's leading international exhibition for electronic automation and test, from system level hardware and software implementation ...

20 [Core-Based Testing of Multiprocessor System-on-Chips Utilizing Hierarchical Fun](#)

Fawzi Azmadi Hussin, Tomokazu Yoneda, Alex Orailoglu, Hideo Fujiwara

January 2007 ASP-DAC '07: Proceedings of the 2007 conference on Asia South Pacific des  
automation

Publisher: IEEE Computer Society





Full text available:  Pdf (224.15 KB)Additional Information: [full citation](#), [abstract](#), [index terms](#)

Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 26, Citation Count: 1

An integrated test scheduling methodology for multiprocessor System-on-Chips (SOC) functional buses for test data delivery is described. The proposed methodology handles single processor SOC and hierarchical bus multiprocessor ...

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